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Review on suitable eDRAM configurations for next nano-metric electronics era

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We summarize most of our studies focused on the main reliability issues that can threat the gain-cells eDRAM behavior when it is simulated at the nano-metric device range has been collected in this review. So, to outperform their memory cell counterparts, we explored different technological proposals and operational regimes where it can be located. The best memory cell performance is observed for the 3T1D-eDRAM cell when it is based on FinFET devices. Both device variability and SEU appear as key reliability issues for memory cells at sub-22 nm technology node.

Keywords : eDRAM, FinFET, sub-Vt, SEU, reliability